PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

TAKAO MASHIMA et al.

Application No.: 10/826,470

Filed: April 16, 2004

For: INFORMATION PROCESSING SYSTEM AND INFORMATION PROCESSING METHOD

Customer No.: 20350

Examiner: Unassigned

Technology Center/Art Unit: 2182

Confirmation No.: 1499

PETITION TO MAKE SPECIAL FOR NEW APPLICATION UNDER M.P.E.P. § 708.02, VIII & 37 C.F.R. § 1.102(d)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is a petition to make special the above-identified application under MPEP § 708.02, VIII & 37 C.F.R. § 1.102(d). The application has not received any examination by an Examiner.

(a) The Commissioner is authorized to charge the petition fee of $130 under 37 C.F.R. § 1.17(i) and any other fees associated with this paper to Deposit Account 20-1430.

(b) All the claims are believed to be directed to a single invention. If the Office determines that all the claims presented are not obviously directed to a single invention, then Applicants will make an election without traverse as a prerequisite to the grant of special status.

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(c) Pre-examination searches were made of U.S. issued patents, including a classification search and a key word search. The classification search was conducted on or around March 29, 2005 covering Class 707 (subclass 10), Class 709 (subclasses 203, 223, and 225), and Class 711 (subclasses 113 and 114), by a professional search firm, Lacasse & Associates, LLC. The key word search was performed on the USPTO full-text database including published U.S. patent applications. The inventors further provided three references considered most closely related to the subject matter of the present application (see references #5-7 below), which were cited in the Information Disclosure Statement filed with the application on April 16, 2004.

(d) The following references, copies of which are attached herewith, are deemed most closely related to the subject matter encompassed by the claims:

(1) U.S. Patent Publication No. 2003/0236884 A1;

(2) U.S. Patent Publication No. 2004/0049572 A1;

(3) U.S. Patent Publication No. 2004/0210656 A1;

(4) U.S. Patent Publication No. 2005/0033804 A1;

(5) Japanese Patent Publication No. JP 09-062499;

(6) Japanese Patent Publication No. JP 08-221309; and

(7) Japanese Patent Publication No. JP 2003-131897.

(e) Set forth below is a detailed discussion of references which points out with particularity how the claimed subject matter is distinguishable over the references.

A. Claimed Embodiments of the Present Invention

The claimed embodiments relate to an information processing system and an information processing method suitable for use with a RAID (Redundant Arrays of Independent Disks) device, for example. More specifically, the present invention allows exchange (updating) of micro programs provided in a processor of an input/output port of a storage device forming an information processing system, to be carried out with good efficiency, without halting application tasks on the host computer.

Independent claim 1 recites an information processing system, comprising a host computer having a plurality of adapters; a storage device having a plurality of host side ports connected to the host computer; a plurality of processors for controlling the plurality of host side ports; a cache memory, connected to the plurality of host side ports, for temporarily holding data in response to commands from the host computer; a shared memory for accumulating information relating to an internal composition of the storage device for reference by the plurality of processors; and an internal management device for outputting the compositional information to an external device; and a management server connected respectively to the internal management device and the host computer, by a communications circuit. The host computer executes a path switching program, and establishes communications paths between the plurality of adapters and the plurality of host side ports. The storage device accumulates information relating to the communications paths, in the shared memory, and the internal management device refers to the information relating to communications paths and judges whether or not communications paths from the plurality of adapters to the cache memory can be secured in the event of at least one of the processors being blocked off. If a judgment result of the internal management device is that the communications paths can be secured, then the internal management device sends a notification indicating that it is possible to block off the processors for which the judgment was made, to the management server, via the communications circuit.

Independent claim 3 recites an information processing method for a host computer, a storage device, and a management server; the host computer including a plurality of adapters; the storage device having a plurality of host side ports connected to the host computer, a plurality of processors for controlling the plurality of host side ports, a cache memory connected to the plurality of host side ports for temporarily holding data in response to commands from the host computer; the management server connected respectively to the storage device and the host computer by a communications circuit. The information processing method comprises judging whether or not communications paths from the plurality of adapters to the cache memory can be secured in the event of at least one of the processors being blocked off, based on information relating to communications paths from the plurality of adapters to the plurality of host side ports; and sending a notification to the management server via the communications circuit, if it is judged that the communications

paths can be secured, indicating that it is possible to block off the processor for which the judgment was made.

One of the benefits that may be derived is that it is possible to exchange micro programs by blocking off processors at a plurality of host side ports of the storage device, in a successive fashion, and hence the micro programs of the storage device can be exchanged without halting operation. Therefore, it is possible readily to overcome the problems associated with a conventional device, namely, the fact that it has been necessary to provide surplus composition, such as spare ports, or the like, in order to exchange micro programs without halting the operation of the storage device, and the fact that exchanging programs requires manual work and this work cannot be automated in a conventional device.

B. Discussion of the References

1. U.S. Patent Publication No. 2003/0236884 A1

The patent application publication to Yamamoto et al (2003/0236884 A1) provides for a Computer System and a Method for Storage Area Allocation. Discussed is a plurality of computers 11a, 11b connected to storage subsystems 12a, 12b via FC switch 18. Storage management server 13 retains configuration information gathered from host 11, storage subsystems 12F, 12c, FC switch 18, and NAS 17 via IP network 142. Storage subsystems 12F, 12c are storage devices provided with a plurality of ports 123 connected to host 11 or file server 19. Cache memory 132 located in storage subsystems 12F, 12c temporarily stores the data read out from disk unit 121 and the data received from host 11. If I/F 112 of host 11 is connected to port 123 of storage subsystem 12F via switch 18, host 11 is judged as not accessible to storage subsystem 12F if access between the two ports is prohibited due to zoning. Storage management server 13 may choose storage subsystem 12 which meets the device requirements presented by requester host 11. If a logical device meets the device requirements, storage subsystem 12F changes status entry 8 in the corresponding logical device management table to "online" and defines the LUN to port 123 reachable from interface 12 of requester host 11. Logical device information about the allocated logical device is sent to storage management device (step 604). See Figures 1 and 6; paragraphs [0024], [0026], [0028], [0033], [0099], [0100], [0110], and [0111].

This reference discloses a computer system having different kinds of storage devices, but does not teach a plurality of processors for controlling a plurality of host side ports. It fails to disclose judging whether or not the communications paths from a plurality of adapters to the cache memory can be secured in the event of at least one of the processors being blocked off; and sending a notification to the management server via the communications circuit, if it is judged that the communications paths can be secured, indicating that it is possible to block off the processor for which the judgment was made, as recited in independent claims 1 and 3.

2. U.S. Patent Publication No. 2004/0049572 A1

The patent application publication to Yamamoto et al. (2004/0049572 A1), assigned to Hitachi, Ltd., provides for Event Notification in Storage Networks. Disclosed is SAN system 200 including storage system 202, SAN switch 204, plurality of servers 206a, 206b, management server 208, and management network 210. Storage subsystem includes a plurality of disk ports 214a, 214b and a plurality of caches 218a, 218b. Disk ports 214a, 214b are connection ports to SAN switch 204 to transfer and receive data to and from servers 206a, 206b. A device that is experiencing a problem issues an SNMP Trap message to manager 502. Manager 502 can determine the cause of the problem and the consequent effects of the event or problem in SAN 200. If failure occurs at switch port 304a of SAN switch 204, manager 502 can determine that an event message has been received because of switch port 304a's failure and that this failure affects server 206a from accessing logical device v1. A trap message 812 is transmitted to manager 502 in response to failure of a disk drive in storage subsystem 202. Manager 502 sends an event notification to the network administrator providing information about the failure of disk drive dd1 and server 206a's inability to access logical device v1. See Figures 2a, 3a, and 5a; paragraphs [0039], [0040], [0057], [0059], and [0062].

This reference discloses a network manager including an event dictionary to interpret an event message received from a device experiencing failure. It does not, however, teach judging whether or not the communications paths from a plurality of adapters to the cache memory can be secured in the event of at least one of the processors being blocked off; and sending a notification to the management server via the communications circuit, if it is

judged that the communications paths can be secured, indicating that it is possible to block off the processor for which the judgment was made, as recited in independent claims 1 and 3.

3. U.S. Patent Publication No. 2004/0210656 A1

The patent application publication to Beck (2004/0210656 A1), assigned to Silicon Graphics, Inc., provides for Failsafe Operation of Storage Area Network. Discussed is a cluster computing system that includes nodes 22, 24, 26 that are connected to disk drives 28 via Fibre Channel switches 30. Nodes 22, 24, 26 are also connected via local area network (LAN) 34. IRIX node 22b is a metadata server for nodes 22, 24, 26. To maximize the speed with which data is accessed, data on disk 28 is cached at the nodes 22, 24, 26 as much as possible. A cluster configuration database can be maintained that associates each port on switch 30 with the host bus adapter (HBA) and client node 22, 24, 26 connected to that port. Zoning commands on switch 30 can disable/enable ports or isolate node 22, 24, 26 from a SAN. Higher level software layers do not need to know the details of the lower level implementation regarding which technique is used to prevent node 22, 24, 26 not communicating with other nodes in the cluster from performing input/output to storage devices 28, 38 via switches 30 connected to node 22, 24, 26. In the case of "raising a fence", i.e., disabling one or more ports on one or more switches 30, a new membership can be formed with the remaining members of the cluster. The surviving cluster can continue with minimal interruption while the failed node(s) 22, 24, 26 recover and eventually rejoin the cluster membership. See Figures 2, 3, and 8; paragraphs [0040], [0045], [0067], [0071], and [0095]-[0097].

This reference discloses disabling port(s) on the switches connected to a failed node to prevent the node from accessing storage devices shared by then odes in a cluster of computer system nodes. It does not, however, teach judging whether or not the communications paths from a plurality of adapters to the cache memory can be secured in the event of at least one of the processors being blocked off; and sending a notification to the management server via the communications circuit, if it is judged that the communications paths can be secured, indicating that it is possible to block off the processor for which the judgment was made, as recited in independent claims 1 and 3.

4. U.S. Patent Publication No. 2005/0033804 A1

The patent application publication to Iwami et al. (2005/0033804 A1) provides for a Storage System. Discussed are host computer 100, switch 120, storage 130, and external storage 180, which are connected to management server 110 through IP network 175. Host computer 100 is provided with at least one port 107 which transmits and receives data to and from storage 130 through network 176. Ports 121 on switch 120 are connected to ports 107 of host computer 100 through IP network 176 or with ports 141 of storage 130 through IP network 177. Cache adapter 150 located in storage 130 includes control memory 155. When control information stored in memory 155 disappears, host computer 100 or NAS unit 145 becomes unable to access the data stored in disk device 157 belonging to cache adapter 150. In case port 141 of NAS unit 145 or protocol adapter 140 fails, storage 130 continues the programs by using alternate NAS unit 145 or port 141. Configuration manager 160 having detected or been notified from another portion of a failure of port 141 or NAS unit 145 judges (steps 2001, 2002) whether the detected or notified failure is the port failure or NAS unit 145 failure. In case entry 1705 is not in the "communicable" status, manager 160 copies the MAC address, the IP address list, the access mode and so on of the port 141 having failed to the individual entries of the port management information corresponding to the alternate port. Manager 160 instructs (at step 2003) the adapter 140 to update the port management information. Manager 160 notifies (step 2005) management terminal 190 of the port management information and the NAS management information. Terminal 190 fetches (at step 2006) the updated information and outputs a complete report to the requester such as management server 110. See Figures 1 and 20; paragraphs [0037], [0039], [0041], [0048], [0051], [0193], [0194], [0195], and [0197].

This reference discloses a management server that issues a reconfiguration instruction of the corresponding relation between the address assigned to the I/F processor and the NAS unit, to the storage system so that the reconfiguration can be made to distribute the processing load and to inherit the processing when a failure occurs. It does not, however, teach judging whether or not the communications paths from a plurality of adapters to the cache memory can be secured in the event of at least one of the processors being blocked off; and sending a notification to the management server via the communications circuit, if it is

judged that the communications paths can be secured, indicating that it is possible to block off the processor for which the judgment was made, as recited in independent claims 1 and 3.

5. Japanese Patent Publication No. JP 09-062499

This reference discloses a program file updating device to provide a file update decision function for replacing a control microprogram during the continuation of online operation and preventing fault occurrence due to the update of the control microprogram and a function which speedily puts the microprogram back to its old version in case of fault occurrence. While processors 21 to 23 operate continuously, a processor 20 is shut down and a control microprogram stored in a new program area 31 of an auxiliary storage device 30 is loaded into the processor 20, which is restored. Similar processes are repeated for the processor 21 to 25 and the programs on all the processors can e updated while the online operation is carried on. When a new microprogram is installed from a floppy disk drive 33, the versions of the control microprograms running on the processors 20 to 25 are decided and their program consistently is checked.

As discussed in the present application at page 2, lines 7, this reference discloses that data transfer is performed smoothly by removing concentration on restricted paths and employing two or more connecting path systems between the host computer and the storage device, data being distributed by switching between these paths. It does not, however, teach judging whether or not the communications paths from a plurality of adapters to the cache memory can be secured in the event of at least one of the processors being blocked off; and sending a notification to the management server via the communications circuit, if it is judged that the communications paths can be secured, indicating that it is possible to block off the processor for which the judgment was made, as recited in independent claims 1 and 3.

6. Japanese Patent Publication No. JP 08-221309

This reference discloses a parallel computer system to quickly and surely transfer file data in which updated data is stored in a parallel computer system which performs the reference and update of data. A central processing unit 2 for control is connected to plural central processing units 3 with a fast coupling device 1, and after input data on which consecutive numbers are attached are stored in a disk device 61 for

intermediate file connected to the central processing unit 2 for control, they are compared with the consecutive numbers of a data consecutive number managing table 10 provided in each disk controller 5, and only a coincident one is stored in a file 82 for updating. Also, a logical pas 14 for reference between the disk controller 5 and a disk device 62 and a logic pass 15 for updating are switched to an alternate pass 16 for updating and an alternate pass 17 for reference, respectively, and a large amount of input data are quickly stored without giving influence to reference processing, and also, the latest file for reference is generated.

As discussed in the present application at page 2, lines 8-12, this reference discloses that in a device having a plurality of processors, micro programs are exchanged in a state one of the processors is blocked off, and the other processors are operating. However, the host computer application connected to the processor that is blocked off will be halted and the tasks must be carried out manually (page 5, lines 9-12).

The reference fails to teach judging whether or not the communications paths from a plurality of adapters to the cache memory can be secured in the event of at least one of the processors being blocked off; and sending a notification to the management server via the communications circuit, if it is judged that the communications paths can be secured, indicating that it is possible to block off the processor for which the judgment was made, as recited in independent claims 1 and 3.

7. Japanese Patent Publication No. JP 2003-131897

This reference discloses a storage with built-in port to reduce the load on a storage system controller for purchasing an exchange PASS software or stopping and starting a server, by realizing the exchange of a MICRO program without stopping the server by shortening the time when a storage port cannot respond. In the storage under SAN environment, more than one spare port is set. When the MICRO program of the port provided to the storage is exchanged, attributive information belonging to the port is copied to the spare port and the connection to the server and the storage is switched to the spare port.

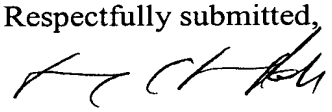
As discussed in the present application at page 1, lines 20-25, this reference relates to a spare port designated exclusively for use during exchange in order to exchange micro programs without halting operation. However, providing a spare port in this manner means providing surplus constituent elements, and the connections to the host computer, as

well as the connections within the RAID, become more complicated. Furthermore, even if a spare port of this kind is used, the task of switching ports, and the like, is carried out manually, and therefore, significant labor, cost and the like, is required in order for a service engineer or a storage administrator to carry out tasks in the location in which the RAID device is situated. Page 4, line 22 to page 5, line 4.

The reference fails to teach judging whether or not the communications paths from a plurality of adapters to the cache memory can be secured in the event of at least one of the processors being blocked off; and sending a notification to the management server via the communications circuit, if it is judged that the communications paths can be secured, indicating that it is possible to block off the processor for which the judgment was made, as recited in independent claims 1 and 3.

(f) In view of this petition, the Examiner is respectfully requested to issue a first Office Action at an early date.

Respectfully submitted,



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